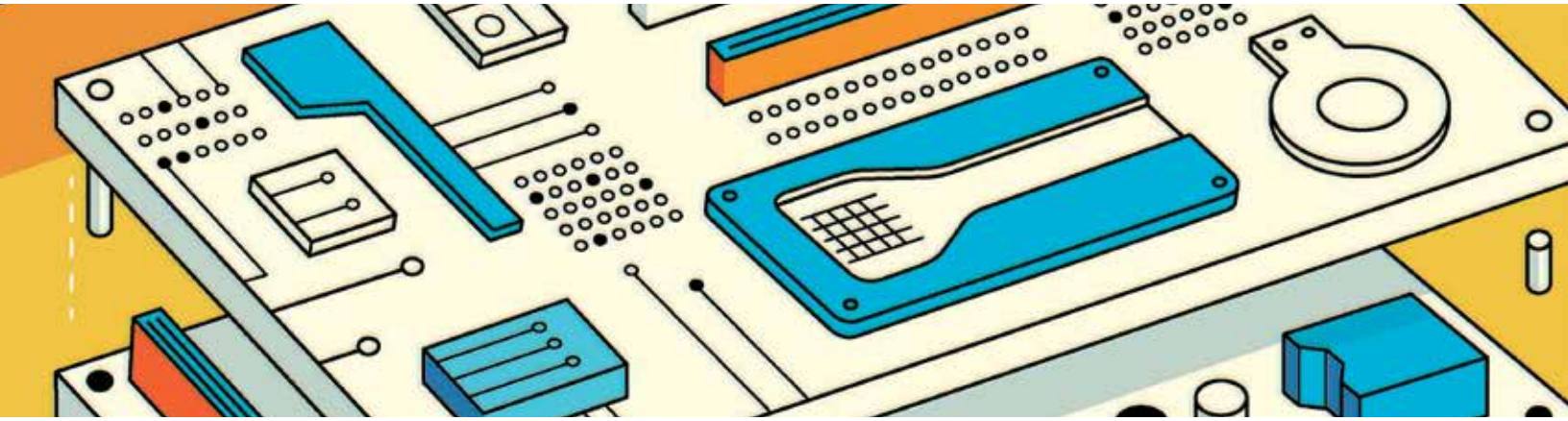


Harry Campbell

What happens when chip-design complexity outpaces development productivity?

Among the forces reshaping the semiconductor industry, few are more important than R&D productivity's inability to keep pace with the challenges of product development. However, there are steps companies can take to close the gap.

Ron Collett and Dorian Pyle

Driven by the market's huge demand for more functionality, performance, and bandwidth, semiconductor-development organizations race to pack as much capability as possible into their integrated-circuit designs. As a result, product development in the semiconductor industry has become a game of leapfrog, whereby competitors do everything possible to raise the bar on time-to-market and product functionality and performance.

Many companies mask problems of design complexity and time-to-market pressures by adding more engineers to project teams. This raises R&D expenditures until they bump up against the constraints of the company's business model. Ramping up head count in lieu of necessary productivity improvements increasingly puts chip makers in a corner; they literally cannot afford to compete in certain chip categories, given the R&D cost.

The good news is that the destructive cycle of productivity chasing the complexity demanded by a hungry market can be broken. To do so requires world-class product-development capabilities. Elements of a successful program go beyond traditional performance-improvement techniques. They include the creation of a robust R&D analytics environment that boosts productivity by ensuring project plans are optimized given the project's complexity, time-to-

market requirements, and budget constraints; improved embedded-software-development capabilities; and a strategic approach to intellectual-property (IP) licensing. Companies that master this set of competencies will have what it takes to survive and prosper in the years ahead.

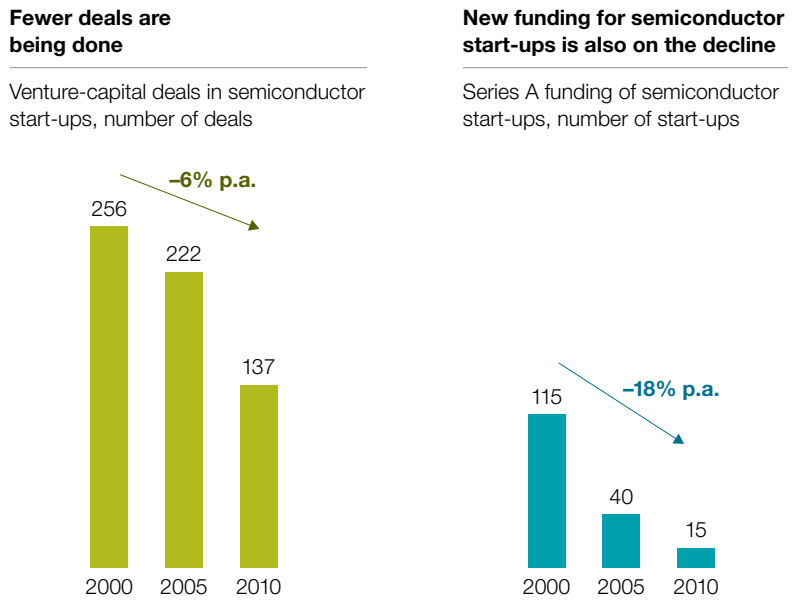
A shifting landscape

Competitive advantage in the semiconductor industry is increasingly achieved more through product-development capabilities than through manufacturing. The reason is simple. Many chip makers that traditionally were vertically integrated are shedding their fabrication plants, or fabs, and outsourcing chip fabrication. Furthermore, some companies that never owned fabs, such as Broadcom and Qualcomm, have become industry leaders. In the absence of manufacturing differentiation, semiconductor players that design the most functionality and performance into their products in the shortest amount of time wield distinct competitive advantage. That puts product-development productivity at center stage.

The problem, however, is that productivity is not keeping pace with the growth in logic and circuit-design complexity. Designing, verifying, and validating chip designs has become enormously complex, especially system-on-a-chip (SOC) devices that integrate processors, analog circuits, memory, and logic and

Exhibit 1

Venture-capital funding is declining for semiconductor start-ups.



Source: Capital IQ; National Venture Capital Association; interviews; McKinsey analysis

Exhibit 2

Several elements are characteristic of R&D excellence.

- **Projects must finish on time, within budget, and to specifications**
- **Companies must achieve best-in-class levels on product-development key performance indicators**
  - Highest development productivity and throughput
  - Shortest project duration (time to market)
  - Highest schedule predictability
  - Lowest product-development cost, including lowest cost per unit of development output
  - Maximum number of products released per year that meet revenue/margin targets
- **The product-development road map must be rationalized given the R&D organization's development capacity**

increasingly demand enormous amounts of software.

Indeed, chip development requires very careful evaluation of the investment given the costs involved. Creating a complex SOC from start to finish[1] while meeting tight market windows demands significant investment and focus on timelines. Complex integrated-chip designs now exceed $100 million, with designs of $20 million to $50 million becoming commonplace among more standard or basic components. Naturally, these rising costs have far-ranging implications for the industry's structure, participants, and value chain.

Consider a $100 million development investment. Its business case typically demands *at least* a $500 million return. If it is assumed that first-mover advantage yields a maximum of 25 to 50 percent market share, then the total market size must be at least $1 billion to $2 billion. Few market segments are that big. Economic considerations such as this are among the reasons players need to thoroughly analyze where to invest.

The same holds true for professional investors. The risk-adjusted return of semiconductor investments no longer meets the threshold most venture capitalists demand. Exhibit 1 shows the decline in venture-capital investment in semiconductor companies during the past ten years.

Product development: The dominant battlefield

Soaring fab costs have made product-development capabilities an important differentiator in the semiconductor industry. As the cost of building and equipping a leading-edge fab climbs above $5 billion, few companies can afford the investment. Not surprisingly, many traditional integrated device manufacturers are now leveraging third-party foundries. Likewise, many are joining—or have already joined—the ranks of the "fab lite" or fabless.

For all semiconductor companies, but especially for fab-lite and fabless players, achieving R&D excellence is no longer a luxury but rather a necessity. Establishing product-development superiority demands harnessing the full

[1] The definition of start is "start of concept investigation," and finish means "release to production."

power of the R&D organization—and time is of the essence. Only with world-class product-development capabilities can semiconductor companies hope to survive the industry's continuing shakeout. Exhibit 2 summarizes the enablers of R&D excellence.

Product-development productivity is the foundation of R&D excellence. It translates into fast time to market, competitive development cost, on-time schedule performance, and high schedule predictability. Yet a serious problem exists: productivity is not keeping up with rising development and design complexity. Average complexity in the semiconductor industry is increasing 4.6 percent faster annually than average development productivity. This is observed by measuring the increase in complexity relative to the increase in productivity during a prior ten-year window. Exhibit 3 shows the relative change. The impact will be significant and disruptive.

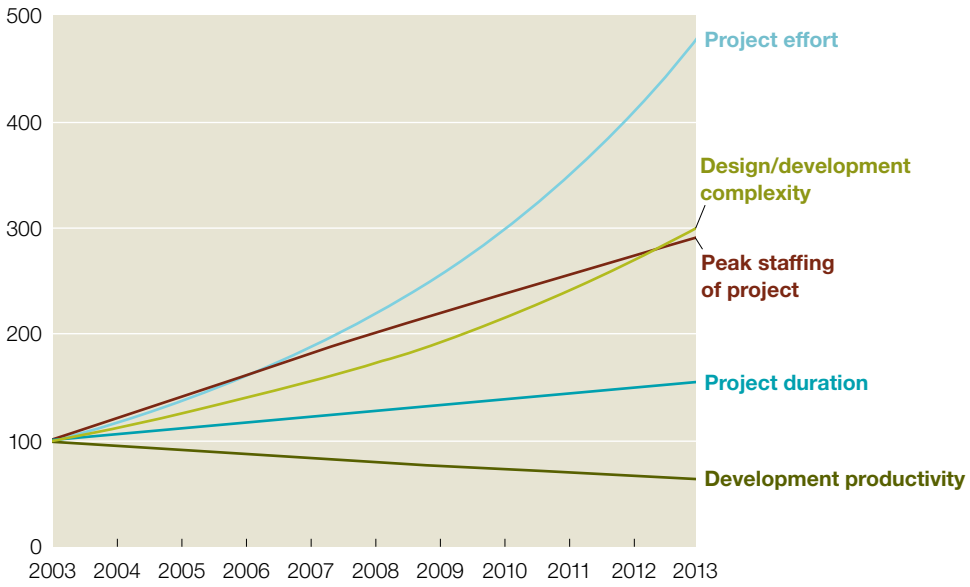
Productivity: Rising but falling

Productivity is rising year over year, but not relative to complexity, which is outpacing it (see sidebar, "The difference between absolute and relative productivity"). We define (and rigorously quantify) design complexity as the level of difficulty, or challenge, in developing a semiconductor product from start to finish. That means from the start-of-concept investigation to a product's release to production manufacturing. It encompasses the entire develop-

Exhibit 3

Average complexity is growing faster than productivity.

% change in trend, 2003 = 100%



ment life cycle, including the so-called fuzzy front end,[2] logic and circuit-design creation and verification, physical design, validation, debug, respins, and qualification. Thus, our complexity metric, which applies to both hardware and embedded software, captures not just the design-creation and implementation challenge but also the full product-development challenge.

Complexity is measured using a production-proven,[3] proprietary set of models that calculate the amount of effort the average development team in the semiconductor industry would expend on developing the particular chip product—from start to finish—given the design's technical characteristics.[4] This is then transformed into a unit of measure called the complexity unit (CU). A calculation of effort underpins the computation, which makes interpretation straightforward. For instance, a two-million-CU design requires, on average, twice as much (total) project effort as a one-million-CU design. Similarly, a six-million-CU design would require three times as much effort as a two-million-CU design, and so on. By calculating the "industry norm effort" for each project, the models yield a statistically defensible and reliable method for determining the relative difference in development complexity, or difficulty, among different chip designs, as seen through the lens of the average development team in the industry.

When the average number of CUs created per person-week (productivity) is compared with the number of CUs that *must be* created to finish a project in the allotted time (to satisfy the time-to-market requirement), a fundamental and persistent mismatch can be observed. Again, complexity is outpacing productivity.

As a secondary check on the analysis, one can examine the average amount of effort expended per integrated-circuit-development project in the past ten years. As Exhibit 3 shows, effort has increased at an annual rate of 17 percent. This offers conclusive evidence that productivity is not keeping pace with complexity (combined with inexorable time-to-market mandates). If productivity were moving in lockstep with rising complexity,[5] team size would remain constant. There would be no reason to increase team size, because teams of constant size would be fully capable of finishing projects in the allotted time. Likewise, if productivity were outpacing complexity, project effort would be falling. Project effort is neither declining nor remaining constant. It is rising, because development organizations have had no choice but to increase team size to ensure competitive cycle times.

Only by increasing team size have semiconductor companies been able to offset the expanding gap between productivity and complexity. At first, the gap was hardly noticeable. However, a persistent 4.6 percent difference compounded annually manifests itself dramatically over time with respect to the need for increasingly larger teams and therefore development cost. Allocating increasing numbers of engineers to projects is an "escape valve" that offsets most of the growing gap between productivity and complexity. Unfortunately, it's becoming an expensive route. During the past ten years, effort for hardware design alone has increased nearly fivefold.

The ballooning cost of product development is a root cause of disruptive change in the industry. A full SOC product family, including platform

[2] The "fuzzy front end" of the product-development process is the period in which the development team formulates a product concept and includes all activities up to the point when the decision is made to invest the resources needed to begin formal development of the product.

[3] The models have been applied successfully to several thousand integrated-circuit projects in the semiconductor and electronics industry.

[4] Examples of technical characteristics include process technology and node, clock speeds/domains, circuit types such as analog/radio frequency, processor cores and memory, functionality of blocks, power consumption, input/output, and amount of reuse per block—hard, soft, test bench, and so on. In short, our model contemplates all parameters that have been shown to have a statistically significant impact on project effort.

[5] Complexity reflects the combined challenge of capturing and implementing the market's requirements *within a specified period of time*. Thus, the complexity metric reflects not only the design's logic/circuit complexity but also the project's schedule, which is dictated by the level of competition (that is, time to market, time to first tape-out, time to samples, time to money, and so on).

The difference between absolute and relative productivity

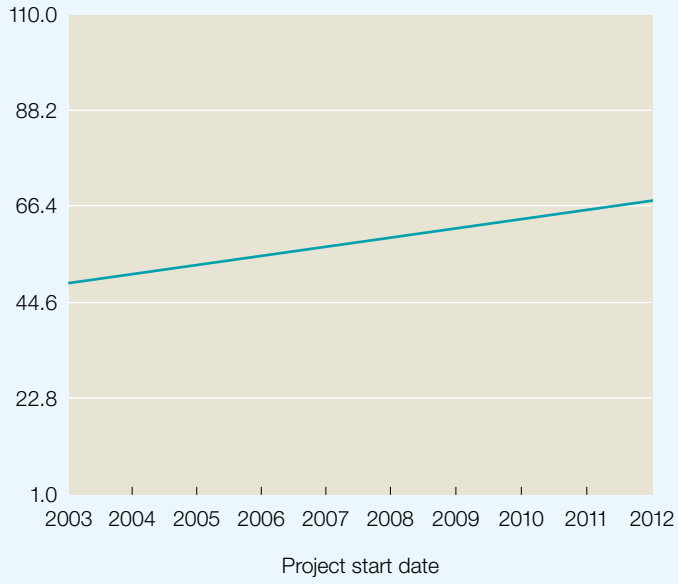
One important element to note is the distinction of relative productivity from absolute productivity. Relative productivity is the change in productivity compared with, or relative to, the change in complexity over a given period of time. Absolute productivity, on the other hand, is the change in productivity measured year on year. Absolute productivity is unmistakably increasing. Consider the effort required to design a million-transistor SOC ten years ago versus what it takes today. There is no comparison—teams expend far less effort now than they did then—which means absolute productivity is rising.

However, relative productivity is declining—even in the face of more design reuse, which has steadily increased during the past ten years, as the exhibit illustrates. Neither the amount of reuse nor reuse-integration efficiency is advancing fast enough to offset the need for larger teams. Once thought of as a potential "silver bullet," reuse has not reduced design complexity enough to close the productivity gap.

Exhibit

Even as design reuse increases, relative productivity has fallen.

Amount of average chip design implemented from preexisting logic/circuitry, % of logical and layout data reused



and derivatives, can cost $150 million or more to develop. A declining number of companies can afford that level of investment.

Justifying large development investments demands an appropriate risk-adjusted return. As development cost has risen, the return has been increasingly difficult to find. There is evidence of this throughout the industry. Many semiconductor organizations that once touted SOC development as their future have significantly scaled back development or withdrawn altogether. Many companies and business units still developing these complex chips are either being absorbed by competitors or selling off their IP and exiting the business. When combined with the shift to outsourced manufacturing, the impact of skyrocketing product-development costs will be a complete restructuring of the economics of the semiconductor industry.

The complexity, productivity, and cost treadmill

Complexity is outpacing productivity as a result of two forces acting in concert. First, the semiconductor market, which is increasingly driven by the consumer, wants more functionality, performance, and bandwidth. It wants more capability in its mobile devices, automobiles, entertainment systems, computers, and peripheral devices. Its thirst for more capability and therefore complexity—at the right price point—is virtually insatiable and spans myriad application segments.

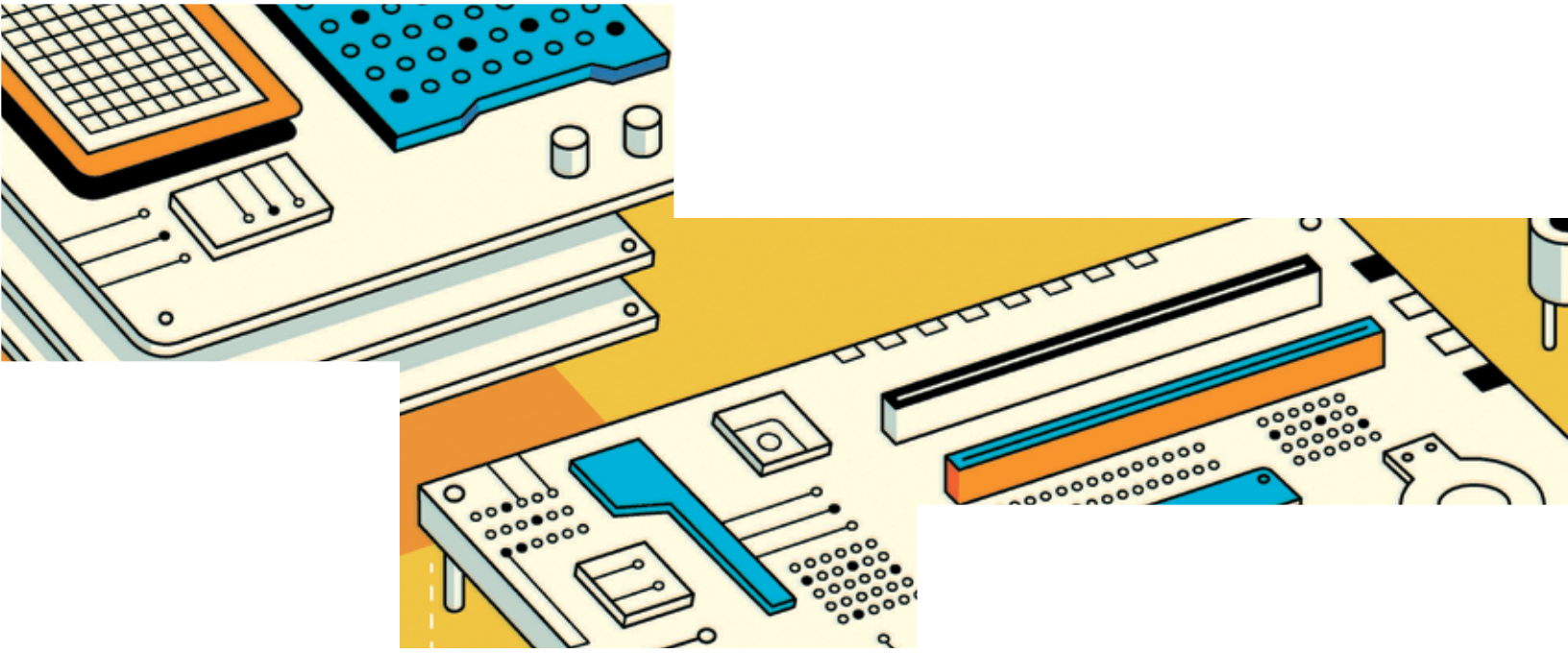
Second, semiconductor competitors aggressively pursuing the global market opportunity recognize they must achieve first-mover advantage with products boasting the most value and differentiation, which invariably demands high complexity. To do this, companies are deploying ever-larger teams to increase development throughput, or rate of output, with the goal of leapfrogging or at least staying even with rivals. The goal, of course, is to introduce winning products faster than competitors. Thus it is the companies themselves causing complexity to outpace productivity by deploying increasingly larger teams to implement more functionality and higher performance chips. Why do they do it? In short, it is because those possessing the financial means *can afford to do it*. Inevitably, as team sizes continue to grow, less well-heeled competitors will drop out of the race. Even financially strong companies are increasingly concluding there are better places to allocate capital. This self-selection process will drive consolidation in each subsegment of the semiconductor industry.

Attacking the gap

Successful semiconductor companies can develop specific capabilities that will allow them to narrow the gap between R&D productivity and product complexity without necessarily making dramatic increases to team size. Such capabilities should provide insights to assess new and road-map projects in a concrete way to rationalize the broader project portfolio. As we noted in last year's issue of *McKinsey on Semiconductors*, aligning product-portfolio and development road maps with market opportunities is a critical enabler.

Cornerstones of a program that narrows the gap include the creation of a robust analytics environment tracking key performance indicators across all dimensions of each design project, especially productivity and throughput[6]; a renewed focus on excellence in embedded-software development; and a robust approach to IP licensing to help deliver silicon on time and on budget.

[6] At key milestones, recalculating the R&D productivity and throughput necessary for the project to finish on time can provide an early indicator of whether the project schedule is likely to slip. For example, if specifications change or engineering resources do not ramp up as planned, the team may be forced to achieve much higher productivity than is realistically possible. Thus, it is quite useful to recalculate at regular intervals the productivity target the team must achieve, especially if major changes to the project occur.



Best-in-class organizations are raising the stakes by taking bold steps to improve R&D productivity dramatically, including leveraging predictive analytics for resource planning and schedule estimation. In so doing, they more reliably match team size to complexity—and in many cases can deploy smaller teams than competitors. On average, companies must improve productivity by 4.6 percent annually to offset the "subsidized" staffing advantage of rivals. The use of advanced analytics and processes that systematically identify product-development bottlenecks is key to making this possible.

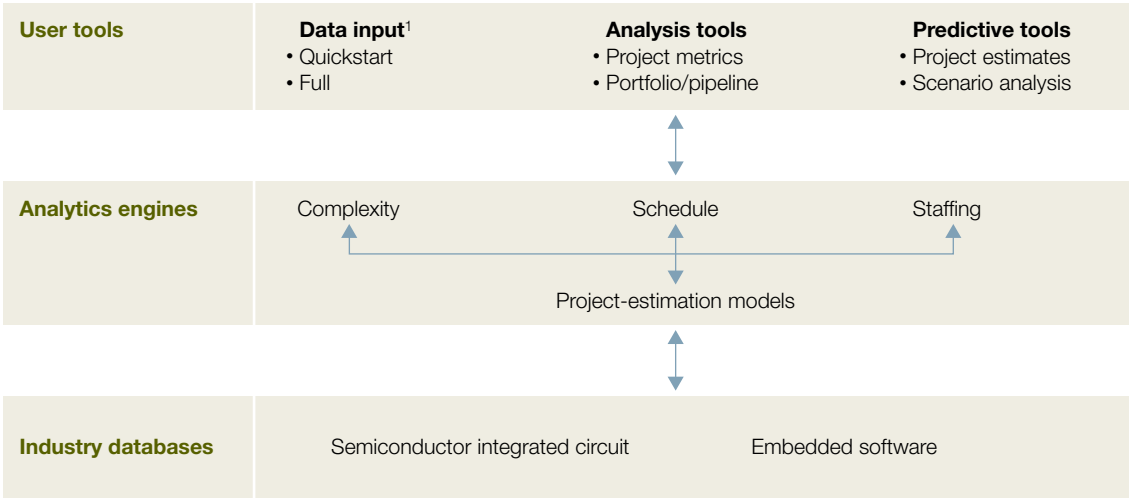
Loss of productivity, budget overruns, and missed schedules frequently stem from a mismatch between the organization's R&D capacity and product-development road map. In short, the R&D organization's resources are often heavily oversubscribed—not enough engineers are available to finish all the projects on time within the road map's target time horizon. Imbalances between R&D capacity and the product-development portfolio are among the most common failure mechanisms from which semiconductor companies suffer.

Underestimating the number of engineering resources to implement the road map is the root cause. Projects are not staffed commensurately with their logic and circuit-design complexity and development-schedule constraints. The lack of a reliable R&D productivity measurement is one reason for this disconnect. A baseline measurement of productivity is therefore the first and most important step in ensuring the product-development road map aligns with the R&D organization's capacity.

Any significant mismatch between capacity and demand must immediately trigger portfolio rationalization. Without robust analytics, getting

Exhibit 4

A robust analytics platform can help companies estimate needed resources.



[1]The data-input environment of an analytics platform can allow users to enter data anywhere along a continuum from a high level of abstraction (quickstart) to a high level of detail (full).

a reliable estimate of resource requirements is extremely difficult. Exhibit 4 illustrates one approach that will yield a fact-based answer, rather than a hunch or gut feeling. Such architecture would track and analyze hundreds, if not thousands, of project parameters, allowing a company to create reliable predictive and estimation models.

In addition to bold R&D improvement initiatives, chip companies are closing the gap between productivity and complexity by shifting from hardware to embedded software to implement functionality and create value. Increasingly, only functionality demanding the highest performance will be implemented in custom hardware. The rest will rely on standard processor cores executing a full software stack. Embedded software can increasingly replace hardware as the vehicle for implementing functionality and creating value given the following advantages:

- Requirements and specifications changes are far less costly and more easily implemented in software than in hardware.
- Product enhancements and upgrades can be implemented more frequently and far less expensively in software.
- Software developers are more readily available globally and typically have lower costs than integrated-circuit engineers.
- Software interfaces enable customers to more easily integrate products into their environments, making them more attractive to customers.

However, despite its many advantages, embedded software is no panacea. Overall performance characteristics will still be determined by hardware. Innovation in chip design remains the foundation of ever-increasing efficiency, speed, and power performance.

A further step semiconductor companies might take to fill the complexity-and-productivity gap is to expand their use of third-party logic and circuit blocks and processor cores, also known as IP. Successful R&D organizations will shift their mind-sets from the historical "let's make it ourselves" to "let's see if can we buy or license it" (at a price point that makes sense).

For many years, IP licensing has been a fragmented industry comprising myriad small, independent suppliers. However, large electronic-design-automation (EDA) vendors are aggressively pursuing the business opportunity, acquiring numerous companies to accelerate their entry. The success of ARM Holdings is not lost on its EDA brethren. ARM demonstrates that it is quite possible to become a large, profitable "silicon-less" semiconductor company.

EDA companies' aggressive pursuit of the IP business is a boon for semiconductor companies, as it enables integrated device manufacturers and fabless suppliers to focus their R&D resources on creating more value-added IP. On the other hand, as the breadth and depth of their IP portfolios expand, EDA vendors themselves become suppliers of added value, which once belonged to semiconductor companies. During this transition, EDA vendors invariably become competitors of the chip companies' internal R&D organizations, much as they did 20 years ago when they displaced the internal computer-aided-design groups of semiconductor companies. This has already begun, and successful semiconductor companies will aggressively restructure their R&D organizations to take advantage of the shift.

• • •

R&D productivity's inability to keep pace with the challenges of product development will be one of the major issues for the industry in the years ahead. The insatiable demand for more functionality, performance, and bandwidth puts heavy pressure on R&D teams. Only companies with world-class product-development capabilities are likely to stay ahead of competitors and market demands.

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