Advanced-packaging technologies: The implications for first movers and fast followers

Adoption of 3-D technologies appears inevitable, creating both opportunities and risks.

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The commercial reality for most integrated-circuit (IC) manufacturers is that node migrations and changes in wafer sizes are slowing down even as capital expenditures are increasing. One way for manufacturers to preserve their edge on their circuits' small sizes, low costs, and high performance is to incorporate newer chip-packaging options such as 2.5-D integrated circuits (2.5DICs) and 3-D integrated circuits (3.0DICs) into their production processes. These advanced-packaging technologies, many of which are still in their infancy, promise greater chip connectivity and lower power consumption compared with traditional packaging configurations.

Given these advantages, their adoption seems inevitable. According to our research, the number of integrated circuits containing 2.5DIC and 3.0DIC technologies is expected to grow tenfold—from about 60 million units in 2012 to well over 500 million in 2016 (Exhibit 1). Meanwhile, advanced packaging has become a technology priority for the Chinese semiconductor industry, according to the high-level policy framework released by the State Council of the People's Republic of China in June 2014. The council aims to have advanced packaging account for about 30 percent of all packaging revenues earned by Chinese vendors by 2015.

But there is still a lot of uncertainty in the market about 2.5DIC and 3.0DIC technologies—for instance, when and how exactly to adopt these newer packaging configurations, who will dominate among the players, and the role China will play. There are significant risks and investments (of time and money) associated with being an early adopter—the first movers will need to help reduce multiple technology standards to only a few, for instance, and will need to reconsider their roles within the manufacturing value chain. Companies in all semiconductor sectors (for instance, memory suppliers, logic producers, foundries, and packaging subcontractors) must explore strategic alliances and partnerships to ensure that a viable ecosystem for advanced packaging develops. For IC manufacturers, foundries, and others, there is also the potential to gain defensible leads in pricing and volume against rivals. Semiconductor players are therefore facing critical decisions when it comes to advanced packaging, choices that will be more or less complex depending on whether they aim to be first movers or fast followers.

Technology and market overview

Before making any strategy or process changes, semiconductor players must consider where the advanced-packaging market has been and where it is going.

The process. For IC manufacturers and foundries, end-stage packaging represents the smallest and least profitable component of the semiconductor manufacturing process (see sidebar, "What is advanced packaging?"). The entire packaging process engenders a series of front-end, middle, and back-end activities that are carried out after the integrated circuit has been designed but before chip testing begins. Critical packaging activities from start to finish include drilling (etching, lithography, and insulation), copper filling of the insulated hole to enable connectivity, grinding the surface of the wafer to expose the copper pillar (also called reveal), bumping the pillar to soften the surface, chip stacking, and chip testing.

IC manufacturers tend to manage many of the front-end activities in this process, but most of the midstage and back-end activities are performed by foundries that specialize in outsourced assembly and testing (OSAT). Compared with the integrated-device-manufacturing (IDM) market, the OSAT market is much more fragmented; the combined sales of the four companies that lead this segment account for only 45 percent of the entire OSAT market. OSAT players have lower profit margins (about 20 percent versus 40 percent for IDMs) and higher material and labor costs, and they primarily compete on operational efficiency rather than innovation.

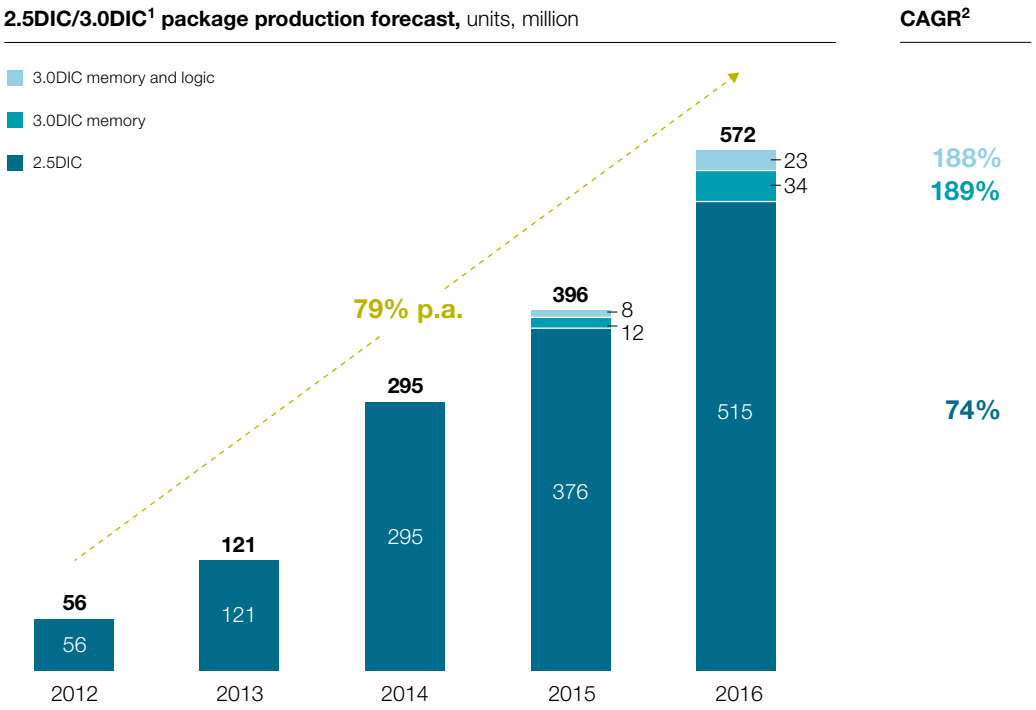
2.0DIC technology. Existing 2-D integrated-circuit (2.0DIC) flip-chip and wafer-level packaging technologies have shown solid growth over the past five years and are used in a number of mainstream applications—predominantly in high-end smartphones (the iPhone and Samsung Galaxy, for instance) and tablets, which must meet stringent size and power-management requirements. Flip-chip packaging involves applying soldered bumps on the top side of a fabricated wafer; the integrated circuit can then be flipped and aligned with grooves on an external circuit to enable the necessary connections. This form of packaging occupies less space in products and offers higher input/output rates, because the whole surface area of the chip can be used for interconnection instead of just the outside edge, as is the case with traditional

wire-bonding methods. In wafer-level packaging, the integrated circuit is packaged while it is still part of the silicon—meaning the package is the same size as the die, and the manufacturing process is streamlined, because conductivity layers and solder bumps are applied to the integrated circuit before dicing occurs.

2.5DIC and 3.0DIC technologies. Emerging 2.5DIC and 3.0DIC technologies promise to extend flip-chip and wafer-level capabilities, enabling multiple dies to be stacked vertically together through the use of interposers and through silicon via (TSV) technology. The TSV stacking technology allows for a greater amount of functionality to be packed into the chip without having to increase its size, and the interposer layer (which essentially performs a routing function) serves to shorten critical electrical paths through the integrated circuit, creating faster input and output. So according to our estimates, an application processor and memory chip encased using advanced-packaging technologies would be about 30 or 40 percent smaller and about two or three

Exhibit 1

2.5DIC and 3.0DIC technologies are growing.



[1]2.5-D integrated circuits/3-D integrated circuits.
[2]Compound annual growth rate. Figures have been rounded up.

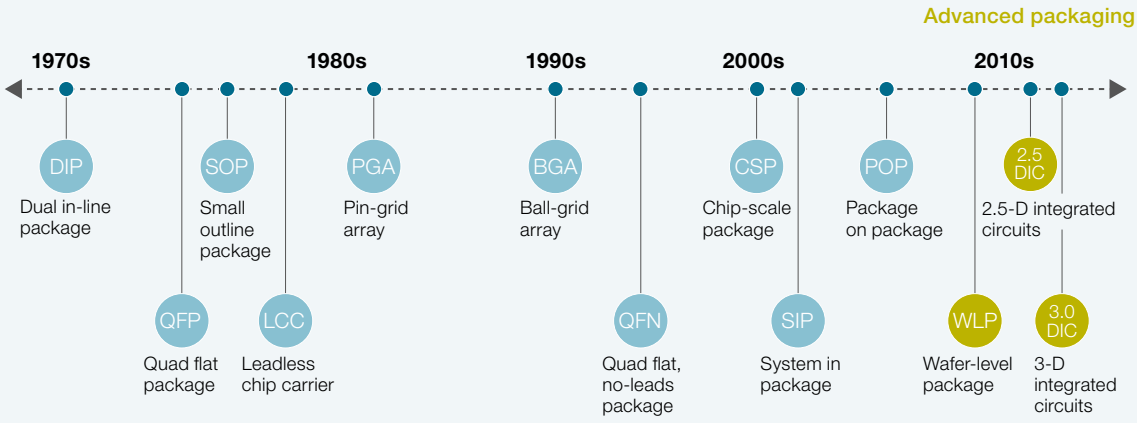
Source: Gartner; New Venture Research; McKinsey analysis

What is advanced packaging?

During the final stages of semiconductor development, a tiny block of materials (the silicon wafer, logic, and memory) is wrapped in a supporting case that prevents physical damage and corrosion and allows the chip to be connected to a circuit board. Typical packaging configurations have included the leadless chip carriers and pin-grid arrays of the 1980s, the system-in-package and package-on-package setups of the 2000s, and, most recently, 2-D integrated-circuit technologies such as wafer-level, flip-chip, and through silicon via setups (exhibit).

Exhibit

Integrated-circuit packaging has evolved since the 1970s.



Source: IC Insights; Yole Développement; McKinsey analysis

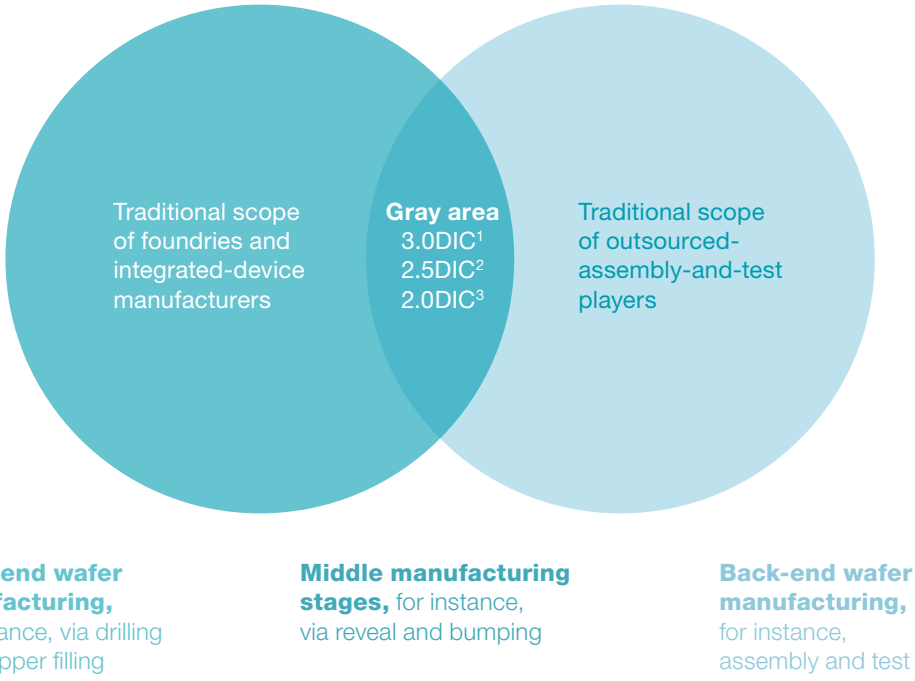
times faster than a chip packaged using older technologies and may create power savings of up to 40 percent or more. Demand for 2.5DIC and 3.0DIC technologies is dependent upon a range of factors, of course, including a thriving market for low-end smartphones, tablets, wearable devices, and other connected consumer goods, as well as an ecosystem in which multiple semiconductor companies (not just a few big players) are committed to upgrading to newer packaging technologies.

How will the market unfold?

The sophistication of 2.5DIC and 3.0DIC technologies, and the economics for the IC manufacturers and OSAT players that produce them, means that IDMs and foundries will still need to handle the front-end work, while OSAT players will remain best suited to handle the back-end processes, such as via reveal, bumping, stacking, and testing. The latter activities rely on interposer manufacturing, a cost-sensitive process with low technical

Exhibit 2

Who owns the gray area?



[1]3-D integrated circuits.
[2]2.5-D integrated circuits.
[3]2-D integrated circuits.

Source: IC Insights; Yole Développement; McKinsey analysis

requirements. But there is a gray area emerging midstream, as Exhibit 2 shows, and IC manufacturers may need to reconsider their role in this stage of production, exploring the trade-offs between taking on higher process and implementation costs and gaining improved performance and competitive advantage through early adoption of 2.5DIC and 3.0DIC technologies.

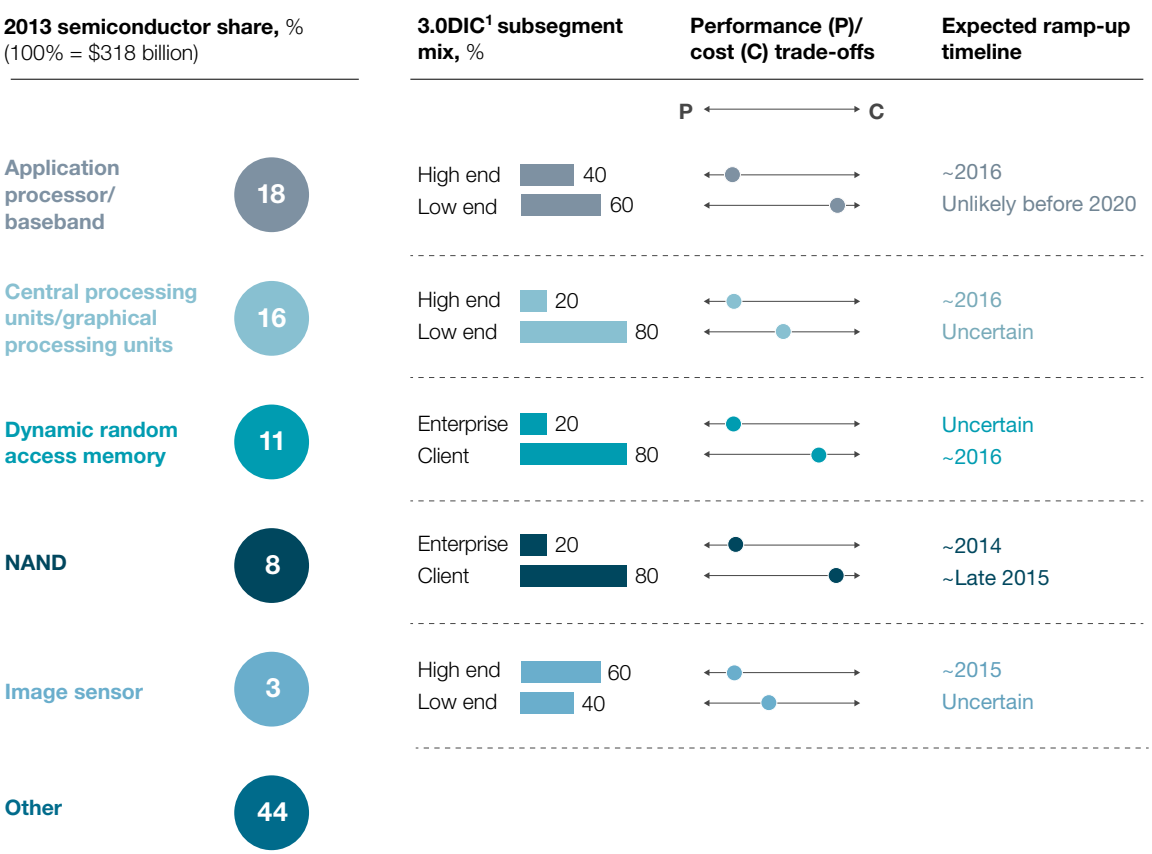
Indeed, the market probably will not move monolithically; different segments likely will make the transition based on the relative benefits of investment and the level of competition. The IDMs and foundries that produce high-end application processors, higher-end image sensors, enterprise memory devices, graphical processing units, and central processing units will likely be among the first to make a move. In fact, some leading-edge graphical processing units and high-end memory products are already in the early-adoption phase. But those that traffic in integrated circuits for lower-end products, such as basebands

for low-end to midrange handsets, will likely transition much later (Exhibit 3). Early adopters would likely include companies such as Intel, Samsung, and Taiwan Semiconductor Manufacturing Company—those with enough scale to drive up volume, bring down costs, and reduce the risk enough so that others will follow suit. Fast followers may then find it easier to make the transition but may also be limited to collaborations with first movers as their only means for capturing cost and performance advantages from advanced-packaging technologies.

For their part, some OSAT foundries are also preparing for a ramp-up to 2.5DIC and 3.0DIC technologies by collaborating with larger foundries to serve fabless players. For instance, Amkor Technology, whose client base includes

Exhibit 3

3.0DIC adoption scenarios vary.



[1] 3-D integrated circuits.

Source: iSuppli; McKinsey analysis

most of the major fabless players across the globe, has been closely working with Xilinx on qualifications relating to TSV technology.

Overall, we believe two adoption scenarios could unfold. First is a slow and steady transition where semiconductor companies would gradually move from flip-chip and 2.0DIC technologies toward incorporating 2.5DIC and 3.0DIC technologies into their chips; the latter technologies would account for between 20 and 30 percent of the advanced-packaging market by 2022, but with only a few big players adopting them and implementation costs that would still be 50 percent higher than 2.0DIC costs. Second is a hard right turn in the industry, where 2.5DIC and 3.0DIC technologies would account for more than 50 percent of the advanced-packaging market by 2022, and multiple industry players would have adopted 3.0DIC technologies and collaborated to strengthen the advanced-packaging ecosystem. Implementation costs would be only 20 to 30 percent higher than those associated with 2.0DIC. A slow and steady transition is more likely, given that production costs are not dropping fast enough and potential end markets for devices that would contain 2.5DIC and 3.0DIC chips (wearables, for instance) have garnered early buzz but have been slow to develop.

Implications for first movers and fast followers

What will it mean to be a first mover in 2.5DIC and 3.0DIC packaging technologies? The early adopters will need to invest significantly in the ecosystem—hiring new engineers, for instance, or spending the time and money to establish partnerships. They will also need to find cost-effective ways to upgrade their equipment to handle newer TSV-based technologies and processes. In some cases, existing 2.0DIC machinery can be expanded to meet newer capacity requirements. But IC manufacturers and foundries may also need to purchase and install new equipment for, say, TSV etching or copper filling. We estimate that in preparation for the shift to advanced-packaging technologies, industry players may invest between $200 million and $300 million on such equipment in 2016. IC manufacturers and foundries could also address this need by entering into partnerships with equipment manufacturers to codevelop bonding, plating, and reveal capabilities that they may not have.

First movers will also need to shape the industry's discussions about packaging standards. Currently, for instance, there is no standard method for temporary bonding and debonding of integrated circuits; different plants use either laser, heat, or

The early adopters will need to invest significantly in the ecosystem and shape the industry's discussions about packaging standards.

mechanical processes to do the same job, thereby missing an opportunity to not only save costs but also minimize quality issues. First movers should consider working with other players in the advanced-packaging industry to establish common process recipes, equipment specifications, logic-to-memory interfaces, and so on. Several such partnerships and initiatives are under way. The semiconductor industry association JEDEC Solid State Technology Association (formerly the Joint Electron Device Engineering Council) for several years has been working toward a standard for the use of 3.0DIC packaging technologies in IC manufacturing. In addition, GLOBALFOUNDRIES has developed the Global Alliance for Advanced Assembly Solutions to accelerate innovation in semiconductor connection, assembly, and packaging technologies; alliance members include Amkor Technology, ASE Group, and STATS ChipPAC in the assembly-and-test area.

For their part, fast followers can mitigate risks and minimize investments as first movers take the lead. As 2.5DIC and 3.0DIC technologies take off, however, fast followers will likely want to get back into the fray. They will need to closely monitor the first movers' activities, participate in discussions regarding standardization, and keep the lines of communication open with customers to gauge their needs in advanced packaging. They may also want to track potential M&A partners—for instance, TSV equipment makers.

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Collaboration among OSAT players, IDMs, foundries, and others in the semiconductor market will be critical for building a reliable advanced-packaging ecosystem—one that recognizes the importance of scale, second-source providers of packaging services (to preserve customer choice), and strategic alliances among memory suppliers, logic IDMs, foundries, and subcontractors. It will be an important factor in allowing companies to optimize their returns on advanced-packaging technologies and ensure continued innovation.

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